COMP2825 – Exercises – Pipelining

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Exercise

We assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Answer the following questions for a non-pipelined processor as well as a pipelined processor.

a. What is the clock cycle time? What is the throughput?

b. What is the latency of an instruction?

c. What is the latency for 100 instructions?

d. What is the speed up for 100 instructions?

Exercise – Solution

a.

non-pipelined processor: clock cycle time = 250 + 350 + 150 + 300 + 200 = 1250 ps

Throughput = 1/clock cycle time = 1/1250 instr/ps

Pipelined processor: clock cycle time = 350 ps (maximum of the latencies for different stages)

Throughput = 1/clock cycle time = 1/350 instr/ps → throughput has increased

Exercise – Solution – Continued

b. For a non-pipelined processor, the cycle time must allow an instruction to go through all stages in one cycle. **The latency of an instruction is the same as clock cycle time** since it takes the instruction one cycle to go from the beginning of FI to the end of WB. Therefore, the latency of an instruction for a non-pipelined processor is 1250 ps.

Pipelining reduces the cycle time to the length of the longest stage. Latency of an instruction becomes **clock cycle time * N** where N is the number of stages as one instruction will need to go through each of the stages and each stage takes one clock cycle. Therefore, for a pipelined processor, the latency an instruction is:

5 x 350 = 1750 ps

Note that although the throughput has increased using pipelining, for a single instruction we have higher latency. But as we know, we use pipelining when we have a number of instructions not only one. Look at the answer to part c.

Exercise – Solution – Continued

c. For a **non-pipelined processor**, we know that each instruction takes one clock cycle time. So, the latency of 100 instructions is calculated as follows:

Total latency = 100 x 1250 = 125,000 ps

Exercise – Solution – Continued

c. For a **pipelined processor**, the latency of 100 instructions is calculated as follows (N is the number of stages):

N x clock cycle time + (the number of instructions - 1) x clock cycle time

→Total latency = 5 x 350 + 99 x 350 = 1750 + 34650 = 36,400 ps → the total latency is less than the latency of the non-pipelined processor

The reason for the above formula:

To have a full pipeline, we must have 5 stages of 5 different instructions running in one clock cycle time. We only reach a full pipeline when the last stage (5^{th} stage) of the first instruction finishes (i.e., after 5 clock cycles). Therefore, one component of the total latency will be 5 x 350. After reaching the full pipeline, then, we need one clock cycle for each of the remaining instructions (99 x 350). You can refer to the following mini example for 10 instructions to observe the above explanation.

Exercise – Solution – Continued

d.

Speedup = latency of the non-pipelined processor/ latency of the pipelined processor

→ Speedup = 125000/36400 = 3.43

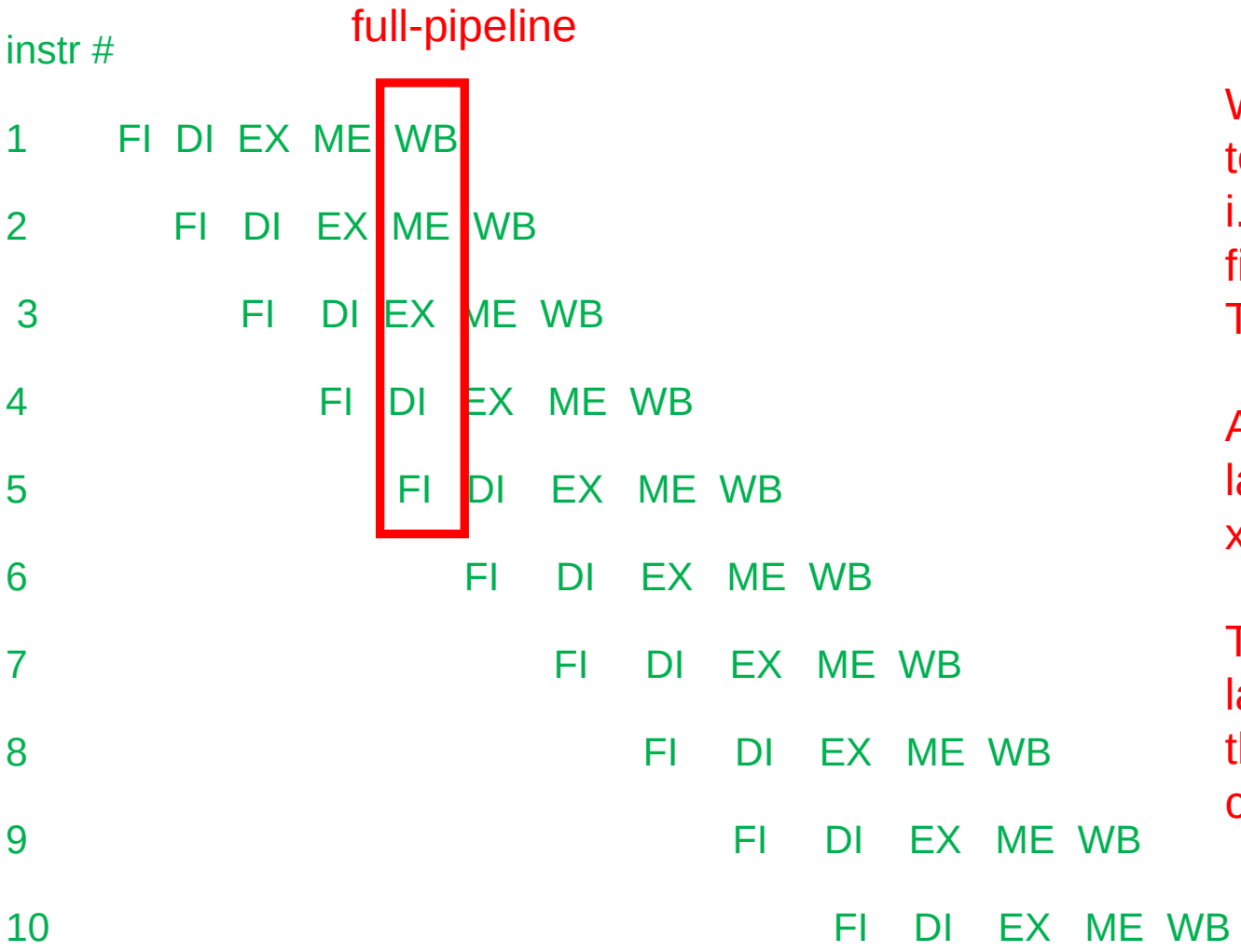
Mini-Example

Compute the latency for 10 instructions. We create the pipeline as follows:

```
instr #
1       FI  DI  EX  ME  WB
2           FI   DI   EX  ME  WB
 3              FI    DI  EX  ME  WB
4                  FI   DI   EX   ME  WB
5                      FI   DI    EX   ME  WB
6                          FI    DI    EX   ME  WB
7                              FI    DI    EX   ME  WB
8                                  FI    DI    EX   ME  WB
9                                      FI    DI    EX   ME  WB
10                                         FI    DI    EX   ME  WB
```

Mini-Example – Continued

Mini example: Compute the latency for 10 instructions. We create the pipeline as follows:



We know that each column corresponds to a clock cycle. We have 14 columns, i.e., in total there are 14 clock cycles to finish the execution of all 10 instructions. Total latency = 14 x 350 = **4900 ps**

Another way to calculated the total latency (the formula we saw in slide 6): 5 x 350 + 9 x 350 = 1750 + 3150 = **4900 ps**

This formula is useful when we have a large number of instructions and drawing the pipeline to get the number of clock cycles would not be possible.